

DOCKET NO. FIS9-2003-0235US1

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:

Haining S. Yang, *et. al.*

Group Art Unit: Unknown

Serial No.: 10/707,841

Examiner: unknown

Filed: 01/16/2004

For: **METHOD AND STRUCTURE FOR CONTROLLING STRESS IN A TRANSISTOR CHANNEL**

Commissioner for Patents  
P.O. Box 1450  
Alexandria, VA 22313-1450

**INFORMATION DISCLOSURE STATEMENT  
UNDER 37 C.F.R. 1.56**

Sir:

Under provisions of 37 C.F.R. 1.97 through 1.99 and pursuant to applicant's duty of disclosure under 37 C.F.R. 1.56, applicants respectfully bring the documents listed on the attached Form PTO-1449 to the attention of the Examiner in charge of the above-identified application. A copy of the non-US patent documents is enclosed for the convenience of the Examiner.

This citation does not constitute an admission that the cited references are relevant or material to the claims nor should it be construed as a representation that no other art than that identified exists. They are merely cited as constituting related art of which the applicant is aware.

It is respectfully requested that these documents be considered by the Examiner and formally made of record in this application.

Respectfully submitted,

Andrew M. Calderon

Reg. No. 38,093

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1750 Tysons Boulevard, Suite 1800  
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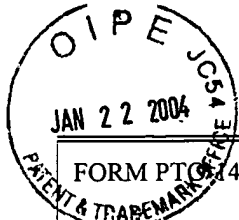
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FORM PTO/SI 449 (Modified)	ATTY. DOCKET NO. FIS9-2003-0235US1	SERIAL NO. 10/707,841
LIST OF PATENTS AND PUBLICATIONS FOR APPLICANT'S INFORMATION DISCLOSURE STATEMENT	APPLICANT: Haining S. Yang, et al.	
(Use several sheets if necessary)	FILING DATE: 01/16/2004	GROUP: Unassigned

## REFERENCE DESIGNATION

## U.S. PATENT DOCUMENTS

EXAMINER INITIALS	DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE (IF APPRO.)
	6,228,694 B1	5/8/2001	Doyle et al.			
	6,406,973 B1	6/18/2002	Lee			
	6,281,532 B1	8/28/2001	Doyle et al.			
	5,683,934	11/4/97	Candelaria			
	6,368,931 B1	4/9/2002	Kuhn, et al.			
	5,310,446	5/10/94	Konishi et al.			
	4,853,076	8/1/89	Tsaur et al.			
	US 2002/0090791 A1	7/11/2002	Doyle et al.			
	US 2002/0074598 A1	6/20/2002	Doyle et al.			
	6,509,618 B2	01/21/2003	Jan et al.			
	6,476,462 B2	11/5/2002	Shimizu et al.			
	6,362,082 B1	3/26/2002	Doyle et al.			
	5,565,697	10/15/96	Asakawa et al.			
	US 2003/0040158 A1	2/27/2003	Saitoh			
	US 2002/0086472 A1	7/4/2002	Roberds et al.			
	6,521,964 B1	2/18/2003	Jan et al.			
	6,506,652	01/14/03	Jan, et al.			

## FOREIGN PATENT DOCUMENTS

DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	TRANSLATION	
					YES	NO

## OTHER ART (Including Author, Title, Date, Pertinent Pages, etc.)

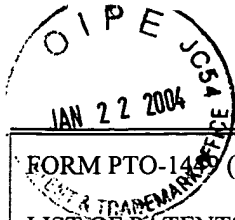
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FORM PTO-1448 (Modified) LIST OF PATENTS AND PUBLICATIONS FOR APPLICANT'S INFORMATION DISCLOSURE STATEMENT (Use several sheets if necessary)				ATTY. DOCKET NO. FIS9-2003-0235US1		SERIAL NO. 10/707/841	
				APPLICANT: Haining S. Yang, et al.			
				FILING DATE: 01/16/2004		GROUP: Unassigned	
REFERENCE DESIGNATION <span style="float: right;">U.S. PATENT DOCUMENTS</span>							
EXAMINER INITIALS		DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE (IF APPRO.)
		5,081,513	1/14/1992	Jackson, et al.			
		3,602,841	8/31/1971	McGroddy			
		6,531,740	3/11/2003	Bosco, et al.			
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		6,501,121	12/31/2002	Yu, et al.			
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		6,361,885	3/26/2002	Chou			
		6,255,169	7/3/2001	Li, et al.			
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		6,165,383	12/26/2000	Chou			
		6,133,071	10/17/2000	Nagai			
		6,046,464	4/4/2000	Schetzina			
		6,025,280	2/15/2000	Brady, et al.			
FOREIGN PATENT DOCUMENTS							
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OTHER ART (Including Author, Title, Date, Pertinent Pages, etc.)							
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(Use several sheets if necessary)		FILING DATE: 01/16/2004	GROUP: Unassigned

## REFERENCE DESIGNATION

## U.S. PATENT DOCUMENTS

EXAMINER INITIALS	DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE (IF APPRO.)
	5,940,736	8/17/1999	Brady, et al.			
	5,880,040	3/9/1999	Sun, et al.			
	5,861,651	1/19/1999	Brasen, et al.			
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	4,665,415	5/12/1987	Esaki, et al.			

## FOREIGN PATENT DOCUMENTS

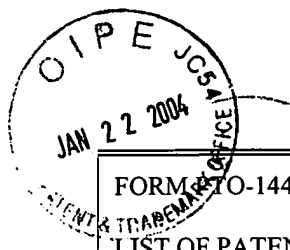
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## OTHER ART (Including Author, Title, Date, Pertinent Pages, etc.)

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FORM PTO-1449 (Modified)	ATTY. DOCKET NO. FIS9-2003-0235US1	SERIAL NO. 10/707,841
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	5,989,978	11/23/1999	Peidous			
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	6,274,444	8/14/2001	Wang			
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	5,557,122	9/17/1996	Shrivastava, et al.			
	5,354,695	10/11/1994	Leedy			
	5,134,085	7/28/1992	Gilgen, et al.			
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	6,319,794	11-20-2001	Akatsu et al.			
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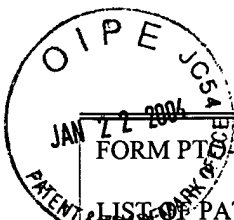
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## OTHER ART (Including Author, Title, Date, Pertinent Pages, etc.)

	Kern Rim, et al., "Transconductance Enhancement in Deep Submicron Strained-Si <i>n</i> -MOSFETs", International Electron Devices Meeting, 26, 8, 1, IEEE, September 1998.
	Kern Rim, et al., "Characteristics and Device Design of Sub-100 nm Strained Si N- and PMOSFETs", 2002 Symposium On VLSI Technology Digest of Technical Papers, IEEE, pp 98-99.
	Gregory Scott, et al., "NMOS Drive Current Reduction Caused by Transistor Layout and Trench Isolation Induced Stress", International Electron Devices Meeting, 34.4.1, IEEE, September 1999.
	F. Ootsuka, et al., "A Highly Dense, High-Performance 130nm node CMOS Technology for Large Scale System-on-a-Chip Application", International Electron Devices Meeting, 23.5.1, IEEE, April 2000.
	Shinya Ito, et al., "Mechanical Stress Effect of Etch-Stop Nitride and its Impact on Deep Submicron Transistor Design", International Electron Devices Meeting, 10.7.1, IEEE, April 2000.
	A. Shimizu, et al., "Local Mechanical-Stress Control (LMC): A New Technique for CMOS-Performance Enhancement", International Electron Devices Meeting, IEEE, March 2001.
	K. Ota, et al., "Novel Locally Strained Channel Technique for high Performance 55nm CMOS", International Electron Devices Meeting, 2.2.1, IEEE, February 2002.

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